Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte DAVID K. LIU
and MAN WONG

Appeal No. 95-2863
Application 08/001,004[1]

ON BRIEF

Before THOMAS, JERRY SMITH, and BARRETT, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 26-29, all the claims pending in the application. The amendment under 37 CFR § 1.116 submitted

[1] Application for patent filed January 6, 1993, entitled "Asymmetrical Non-Volatile Memory Cell, Arrays and Methods for Fabricating Same," which is a division of Application 07/723,700, filed June 25, 1991, now U.S. Patent 5,202,576, issued April 13, 1993, which is a continuation of Application 07/575,105, filed August 29, 1990, now abandoned.

November 4, 1994 (Paper No. 13), has not been entered.

The invention is directed to a method for operating (writing, reading, and erasing) an asymmetric non-volatile memory cell wherein electrons are injected from the source to a floating gate during programming. This is said to overcome problems of "drain side injection."

Claim 26, the sole independent claim, is reproduced below.

26. A method for operating a non-volatile memory cell comprising the steps of:

providing the non-volatile memory cell, wherein said memory cell comprises:

heavily doped source and drain regions formed in a layer of semiconductor, said source and drain regions spaced by a channel region;

a lightly doped source region formed adjacent said heavily doped source region;

a lightly doped drain region formed adjacent said heavily doped drain region;

a floating gate conductor insulatively overlying said channel region and insulatively overlying said lightly doped drain region but not substantially overlying said lightly doped source region; and

a control gate conductor capacitively coupled with said floating gate conductor;

and

programming said non-volatile memory cell by applying a first selected voltage to said control gate, a second selected voltage to said heavily doped source region and a third selected voltage to said heavily doped drain region wherein the application of said selected voltages creates a high electric field adjacent said lightly doped source region thereby injecting electrons from said lightly doped source region onto said floating gate.

The examiner relies on the following prior art reference:

Smayling et al. (Smayling) 4,939,558 July 3, 1990

Claims 26-29 stand rejected under 35 U.S.C. § 103 as being unpatentable over Smayling. The examiner's statement of the rejection is found in the Final Rejection entered May 31, 1994 (Paper No. 9).

OPINION

We affirm-in-part.

Smayling, which is assigned to the assignee of the present application, discloses an asymmetric non-volatile memory cell, which structure appellants admit (Brief, page 7 n.1) is encompassed by claim 26. Smayling has heavily doped source region 18, heavily doped drain region 22, lightly doped source region "reach through" layer 21 adjacent the heavily doped source region, and lightly doped drain region "reach through" layer 21a formed adjacent the heavily doped drain region. A floating gate 35 overlies the channel and overlies the lightly doped source region 21 by a portion 40. A control gate is capacitively coupled (column 2, lines 56-57) to the floating gate conductor. Write, read, and erase modes are described at column 3, lines 22-41.

The examiner finds that the gate in Smayling does not substantially overlie the region 21 (Final Rejection, page 3; Examiner's Answer, page 3). Appellants' arguments regarding claim 26 rely on the difference that the claimed "floating gate

conductor" is "not substantially overlying said lightly doped source region." Thus, appellants "assert that the floating gate 35 substantially overlies the lightly doped source region 21 [in Smayling]" (Brief, page 7) and "the instant claimed invention requires that electrons are injected from the region not underlying the floating gate whereas Smayling et al. disclose programming where electrons are tunneled from the region underlying the floating gate" (Brief, page 7). We agree with the examiner, although some explanation by the examiner would have been helpful in understanding the examiner's interpretation of the claim. The lightly doped source region 21 in Smayling extends all the way underneath the heavily doped source region 18, as shown in figure 3. Although the gate 35 overlies the region 21 by an amount 40, it does not overlie the lightly doped portion 21 to the left of 40, which has a much greater extent. Therefore, the gate is "not substantially overlying" the lightly doped source region 21; "not substantially" is a broad term that does say how much. Claim 26 does not define the structure of the lightly doped source region to be as shown in appellants' figure 1.

Appellants further argue that Smayling teaches "tunneling of electrons across oxide layer 15" (column 3, lines 24-25) and "does not teach the 'injecting' step as required by claim 26" (Reply Brief, page 2). Appellants do not provide definitions of "tunneling" and "injecting." In our opinion, the term

"injecting" is broad enough to cover "tunneling" (i.e., "tunneling" is one kind of "injecting"), especially given the similarities in structures and voltages on the source and gate, between the claimed invention and Smayling.

Appellants do not argue the limitation that the floating gate conductor is "insulatively overlying said lightly doped drain region." Differences not argued are not considered. See 37 CFR § 1.192(c)(6)(iv) (1994). Nevertheless, we note that this limitation is broad because "insulatively overlying" does not specify or imply any certain amount. Figure 3 of Smayling shows some overlap. Appellants state that the gate 35 "does not substantially overlie second reach-through region 21a" (Brief, page 7), which admits that it does partially overlie the region.

For the reasons stated above, we sustain the rejection of claim 26 and dependent claim 28 which is said to stand or fall together with claim 26 (Brief, page 4).

As to the specific voltages of claim 27 (source: 0 volts, drain: 5 volts, gate: 12 volts), we agree with the examiner's position (Examiner's Answer, page 4) that Smayling discloses a similar combination of voltages for programming at column 3, lines 18-32 (source: 0 volts, drain: float, gate: 14 volts). To set a specific voltage, such as 5 volts, instead of a floating voltage on the drain would have been obvious as a matter of

routine selection of operational parameters to one of ordinary skill in the art. Thus, we sustain the rejection of claim 27.

The voltages of claim 29 (source: 0 volts, drain: 1.5 volts, gate: 5 volts) do not correspond to the read voltages in Smayling (source: 5 volts, drain: not mentioned, gate: ± 2 volts), because the source voltage in Smayling is greater than the gate voltage. The examiner has not provided a convincing reason why it would have been obvious to invert the voltages for reading. Accordingly, we reverse the rejection of claim 29.

CONCLUSION

The rejection of claims 26-28 is sustained.

The rejection of claim 29 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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